Introduction to CMOS VLSI Design

Layout, Fabrication, and Elementary Logic Design
CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched

- Define active areas
- Etch and fill trenches
- Implant well regions
- Deposit and pattern polysilicon layer
- Implant source and drain regions and substrate contacts
- Create contact and via windows
- Deposit and pattern metal layers
Inverter Cross-section

- Typically use p-type substrate for nMOS transistor
  - Requires n-well for body of pMOS transistors
  - Several alternatives: SOI, twin-tub, etc.

![Diagram of inverter cross-section with labels and layers: SiO₂, n+ diffusion, p+ diffusion, polysilicon, metal1.

- nMOS transistor
- pMOS transistor
- p substrate
- n well
- GND
- V_DD
- A
- Y

Fabrication and Layout CMOS VLSI Design Slide 3
Well and Substrate Taps

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO$_2$ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO$_2$
Oxidation

- Grow SiO$_2$ on top of Si wafer
  - 900 – 1200 °C with H$_2$O or O$_2$ in oxidation furnace
Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist
Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed
Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step

\[ \text{p substrate} \] \[ \text{SiO}_2 \]
n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO$_2$, only enter exposed Si
Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

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| p substrate | n well |
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Polysilicon

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor
Polysilicon Patterning

- Use same lithography process to pattern polysilicon
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact
N-diffusion

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing
N-diffusion

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion
N-diffusion

- Strip off oxide to complete patterning step
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed
Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires
How transistor looks like
Silicon oxide interface
A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process
Advanced metalization
Advanced metalization
Bonding
Design rules
Intra-Layer Design Rules
Transistor layout
Vias and contacts

1. Metal to Active Contact
2. Metal to Poly Contact
3. Via
4. Metal to Metal Contact
5. Poly to Poly Contact
CMOS inverter layout