**FEATURES**

- **Voltage Noise**
  - 1.1nV/√Hz Max. at 1kHz
  - 0.85nV/√Hz Typ. at 1kHz
  - 1.0nV/√Hz Typ. at 10Hz
  - 35nVp-p Typ., 0.1Hz to 10Hz
- **Voltage and Current Noise 100% Tested**
- **Gain-Bandwidth Product**
  - LT1028: 50MHz Min.
  - LT1128: 13MHz Min.
- **Slew Rate**
  - LT1028: 11V/µs Min.
  - LT1128: 5V/µs Min.
- **Offset Voltage**: 40µV Max.
- **Drift with Temperature**: 0.8µV/°C Max.
- **Voltage Gain**: 7 Million Min.
- **Available in 8-Pin SO Package**

**APPLICATIONS**

- Low Noise Frequency Synthesizers
- High Quality Audio
- Infrared Detectors
- Accelerometer and Gyro Amplifiers
- 350Ω Bridge Signal Conditioning
- Magnetic Search Coil Amplifiers
- Hydrophone Amplifiers

**DESCRIPTION**

The LT1028 (gain of –1 stable)/LT1128 (gain of +1 stable) achieve a new standard of excellence in noise performance with 0.85nV/√Hz 1kHz noise, 1.0nV/√Hz 10Hz noise. This ultra low noise is combined with excellent high speed specifications (gain-bandwidth product is 75MHz for LT1028, 20MHz for LT1128), distortion-free output, and true precision parameters (0.1µV/°C drift, 10µV offset voltage, 30 million voltage gain). Although the LT1028/LT1128 input stage operates at nearly 1mA of collector current to achieve low voltage noise, input bias current is only 25nA.

The LT1028/LT1128’s voltage noise is less than the noise of a 50Ω resistor. Therefore, even in very low source impedance transducer or audio amplifier applications, the LT1028/LT1128’s contribution to total system noise will be negligible.
**LT1028/LT1128**

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage
-55°C to 105°C ................................................ ±22V
105°C to 125°C ................................................ ±16V

Differential Input Current (Note 8) ........................................... ±25mA

Input Voltage ........................................ Equal to Supply Voltage

Output Short Circuit Duration ........................................ Indefinite

Operating Temperature Range
LT1028/LT1128AM, M ........................................... −55°C to 125°C
LT1028/LT1128AC, C ........................................... −40°C to 85°C

Storage Temperature Range
All Devices .............................................. −65°C to 150°C

Lead Temperature (Soldering, 10 sec.) ................................ 300°C

### PACKAGE/ORDER INFORMATION

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<th>ORDER PART NUMBER</th>
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<td>LT1028CS8</td>
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<td>LT1028CS8</td>
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S8 PACKAGE
8-LEAD PLASTIC SOIC

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<td></td>
<td>LT1128MJ8</td>
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<td></td>
<td>LT1128CJ8</td>
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<td>LT1128ACN8</td>
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<td>LT1128CN8</td>
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J8 PACKAGE
8-LEAD CERAMIC DIP

H PACKAGE
8-LEAD TO-5 METAL CAN

N8 PACKAGE
8-LEAD PLASTIC DIP

NOTE: THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGNS

### ELECTRICAL CHARACTERISTICS  \( V_S = \pm 15V, T_A = 25°C, \) unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1028AM/AC</th>
<th>LT1028M/C</th>
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<tbody>
<tr>
<td>( V_{DS} )</td>
<td>Input Offset Voltage</td>
<td>(Note 1)</td>
<td></td>
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<tr>
<td>( \Delta V_{DS} )</td>
<td>Long Term Input Offset Voltage Stability</td>
<td>(Note 2)</td>
<td></td>
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<tr>
<td>( I_{DS} )</td>
<td>Input Offset Current</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
<td></td>
<td></td>
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<tr>
<td>( \epsilon_n )</td>
<td>Input Noise Voltage</td>
<td>0.1Hz to 10Hz (Note 3)</td>
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### ELECTRICAL CHARACTERISTICS  \( V_S = \pm 15V, \ T_A = 25^\circ C, \) unless otherwise noted.

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<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
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<th>LT1128AM/AC</th>
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<th>LT1128M/C</th>
<th>UNITS</th>
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<tbody>
<tr>
<td></td>
<td>Input Noise Voltage Density</td>
<td>( f_0 = 10Hz ) (Note 4)</td>
<td>1.00</td>
<td>1.7</td>
<td>1.0</td>
<td>1.9</td>
<td>nV/√Hz</td>
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<tr>
<td></td>
<td></td>
<td>( f_0 = 1000Hz, ) 100% tested</td>
<td>0.85</td>
<td>1.1</td>
<td>0.9</td>
<td>1.2</td>
<td>nV/√Hz</td>
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<tr>
<td>( I_n )</td>
<td>Input Noise Current Density</td>
<td>( f_0 = 10Hz ) (Note 3 and 5)</td>
<td>4.7</td>
<td>10.0</td>
<td>4.7</td>
<td>12.0</td>
<td>pA/√Hz</td>
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<tr>
<td></td>
<td></td>
<td>( f_0 = 1000Hz, ) 100% tested</td>
<td>1.0</td>
<td>1.6</td>
<td>1.0</td>
<td>1.8</td>
<td>pA/√Hz</td>
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<tr>
<td></td>
<td>Input Resistance</td>
<td>Common Mode</td>
<td>300</td>
<td>300</td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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<td>Differential Mode</td>
<td>20</td>
<td>20</td>
<td>kΩ</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Input Capacitance</td>
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<td>5</td>
<td>5</td>
<td>pF</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>Input Voltage Range</td>
<td></td>
<td>±11.0</td>
<td>±12.2</td>
<td>±11.0</td>
<td>±12.2</td>
<td>V</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Large-Signal Voltage Gain</td>
<td>( R_L \geq 2k, ) ( V_O = \pm 12V )</td>
<td>7.0</td>
<td>30.0</td>
<td>5.0</td>
<td>30.0</td>
<td>V/µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 1k, ) ( V_O = \pm 10V )</td>
<td>5.0</td>
<td>20.0</td>
<td>3.5</td>
<td>20.0</td>
<td>V/µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 600Ω, ) ( V_O = \pm 10V )</td>
<td>3.0</td>
<td>15.0</td>
<td>2.0</td>
<td>15.0</td>
<td>V/µV</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Maximum Output Voltage Swing</td>
<td>( R_L \geq 2k )</td>
<td>±12.3</td>
<td>±13.0</td>
<td>±12.0</td>
<td>±13.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 600Ω )</td>
<td>±11.0</td>
<td>±12.2</td>
<td>±10.5</td>
<td>±12.2</td>
<td>V</td>
</tr>
<tr>
<td>( SR )</td>
<td>Slew Rate</td>
<td>( A_{VCL} = -1 )</td>
<td>11.0</td>
<td>15.0</td>
<td>11.0</td>
<td>15.0</td>
<td>V/µs</td>
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<tr>
<td></td>
<td></td>
<td>( A_{VCL} = -1 )</td>
<td>5.0</td>
<td>6.0</td>
<td>4.5</td>
<td>6.0</td>
<td>V/µs</td>
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<tr>
<td>( GBW )</td>
<td>Gain-Bandwidth Product</td>
<td>( f_0 = 20kHz ) (Note 6)</td>
<td>50</td>
<td>75</td>
<td>50</td>
<td>75</td>
<td>MHz</td>
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<tr>
<td></td>
<td></td>
<td>( f_0 = 200kHz ) (Note 6)</td>
<td>13</td>
<td>20</td>
<td>11</td>
<td>20</td>
<td>MHz</td>
</tr>
<tr>
<td>( Z_O )</td>
<td>Open-Loop Output Impedance</td>
<td>( V_O = 0, \ I_O = 0 )</td>
<td>80</td>
<td>80</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td></td>
<td>7.4</td>
<td>9.5</td>
<td>7.6</td>
<td>10.5</td>
<td>mA</td>
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### ELECTRICAL CHARACTERISTICS  \( V_S = \pm 15V, \ -55^\circ C \leq T_A \leq 125^\circ C, \) unless otherwise noted.

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<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1028AM</th>
<th>LT1128AM</th>
<th>LT1028M</th>
<th>LT1128M</th>
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<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>(Note 1)</td>
<td>30</td>
<td>120</td>
<td>45</td>
<td>180</td>
<td>µV</td>
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<tr>
<td>( \Delta V_{OS} )</td>
<td>Average Input Offset Drift</td>
<td>(Note 7)</td>
<td>0.2</td>
<td>0.8</td>
<td>0.25</td>
<td>1.0</td>
<td>µV/°C</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>( V_{CM} = 0V )</td>
<td>25</td>
<td>90</td>
<td>30</td>
<td>180</td>
<td>nA</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
<td>±40</td>
<td>±150</td>
<td>±50</td>
<td>±300</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td>Input Voltage Range</td>
<td></td>
<td>±10.3</td>
<td>±11.7</td>
<td>±10.3</td>
<td>±11.7</td>
<td>V</td>
</tr>
<tr>
<td>( CMRR )</td>
<td>Common-Mode Rejection Ratio</td>
<td>( V_{CM} = \pm 10.3V )</td>
<td>106</td>
<td>122</td>
<td>100</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td>( PSRR )</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = \pm 4.5V ) to ±16V</td>
<td>110</td>
<td>130</td>
<td>104</td>
<td>130</td>
<td>dB</td>
</tr>
<tr>
<td>( A_{VOL} )</td>
<td>Large-Signal Voltage Gain</td>
<td>( R_L \geq 2k, ) ( V_O = \pm 10V )</td>
<td>3.0</td>
<td>14.0</td>
<td>2.0</td>
<td>14.0</td>
<td>V/µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 1k, ) ( V_O = \pm 10V )</td>
<td>2.0</td>
<td>10.0</td>
<td>1.5</td>
<td>10.0</td>
<td>V/µV</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Maximum Output Voltage Swing</td>
<td>( R_L \geq 2k )</td>
<td>±10.3</td>
<td>±11.6</td>
<td>±10.3</td>
<td>±11.6</td>
<td>V</td>
</tr>
<tr>
<td>( I_S )</td>
<td>Supply Current</td>
<td></td>
<td>8.7</td>
<td>11.5</td>
<td>9.0</td>
<td>13.0</td>
<td>mA</td>
</tr>
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## ELECTRICAL CHARACTERISTICS \( V_S = \pm 15V, \ 0^\circ C \leq T_A \leq 70^\circ C, \) unless otherwise noted.

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<th>LT1128AC</th>
<th>LT1028C</th>
<th>LT1128C</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
<td>(Note 1)</td>
<td>●</td>
<td>15</td>
<td>80</td>
<td>30</td>
<td>125</td>
</tr>
<tr>
<td>( \Delta V_{OS} )</td>
<td>Average Input Offset Drift</td>
<td>(Note 7)</td>
<td>●</td>
<td>0.1</td>
<td>0.8</td>
<td>0.2</td>
<td>1.0</td>
</tr>
<tr>
<td>( I_{OS} )</td>
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<td>( V_{CM} = 0V )</td>
<td>●</td>
<td>15</td>
<td>65</td>
<td>22</td>
<td>130</td>
</tr>
<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
<td>●</td>
<td>±30</td>
<td>±120</td>
<td>±40</td>
<td>±240</td>
</tr>
<tr>
<td></td>
<td>Input Voltage Range</td>
<td>●</td>
<td>±10.5</td>
<td>±12.0</td>
<td>±10.5</td>
<td>±12.0</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>( V_{CM} = \pm 10.5V )</td>
<td>●</td>
<td>110</td>
<td>124</td>
<td>106</td>
<td>124</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = \pm 4.5V ) to ±18V</td>
<td>●</td>
<td>114</td>
<td>132</td>
<td>107</td>
<td>132</td>
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<tr>
<td>AVOL</td>
<td>Large-Signal Voltage Gain</td>
<td>( R_L \geq 2k, \ V_O = \pm 10V )</td>
<td>●</td>
<td>5.0</td>
<td>25.0</td>
<td>3.0</td>
<td>25.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 1k, \ V_O = \pm 10V )</td>
<td>4.0</td>
<td>18.0</td>
<td>2.5</td>
<td>18.0</td>
<td>V/µV</td>
</tr>
<tr>
<td>VOUT</td>
<td>Maximum Output Voltage Swing</td>
<td>( R_L \geq 2k )</td>
<td>●</td>
<td>±11.5</td>
<td>±12.7</td>
<td>±11.5</td>
<td>±12.7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( R_L \geq 600Ω (Note 9) )</td>
<td>±9.5</td>
<td>±11.0</td>
<td>±9.0</td>
<td>±10.5</td>
<td>V</td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current</td>
<td>●</td>
<td>8.0</td>
<td>10.5</td>
<td>8.2</td>
<td>11.5</td>
<td>mA</td>
</tr>
</tbody>
</table>

### Note 1:
Input Offset Voltage measurements are performed by automatic test equipment approximately 0.5 sec. after application of power. In addition, at \( T_A = 25^\circ C \), offset voltage is measured with the chip heated to approximately 55°C to account for the chip temperature rise when the device is fully warmed up.

### Note 2:
Long Term Input Offset Voltage Stability refers to the average trend line of Offset Voltage vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in \( V_{OS} \) during the first 30 days are typically 2.5µV.

### Note 3:
This parameter is tested on a sample basis only.

### Note 4:
10Hz noise voltage density is sample tested on every lot with the exception of the S8 and S16 packages. Devices 100% tested at 10Hz are available on request.

### Note 5:
Current noise is defined and measured with balanced source resistors. The resultant voltage noise (after subtracting the resistor noise on an RMS basis) is divided by the sum of the two source resistors to obtain current noise. Maximum 10Hz current noise can be inferred from 100% testing at 1kHz.

### Note 6:
Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

### Note 7:
This parameter is not 100% tested.

### Note 8:
The inputs are protected by back-to-back diodes. Current-limiting resistors are not used in order to achieve low noise. If differential input currents.

### Note 9:
This parameter is tested on a sample basis only. This parameter guaranteed by design, correlation and/or inference from the slew rate measurement.

### Note 10:
This parameter guaranteed by design, fully warmed up at \( T_A = 70^\circ C \). It includes chip temperature increase due to supply and load currents.

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<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LT1028AC</th>
<th>LT1128AC</th>
<th>LT1028C</th>
<th>LT1128C</th>
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<tbody>
<tr>
<td>( V_{OS} )</td>
<td>Input Offset Voltage</td>
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<td>●</td>
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<td>35</td>
<td>150</td>
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<tr>
<td>( \Delta V_{OS} )</td>
<td>Average Input Offset Drift</td>
<td></td>
<td>●</td>
<td>0.2</td>
<td>0.8</td>
<td>0.25</td>
<td>1.0</td>
</tr>
<tr>
<td>( I_{OS} )</td>
<td>Input Offset Current</td>
<td>( V_{CM} = 0V )</td>
<td>●</td>
<td>20</td>
<td>80</td>
<td>28</td>
<td>160</td>
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<tr>
<td>( I_B )</td>
<td>Input Bias Current</td>
<td>( V_{CM} = 0V )</td>
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<td>±35</td>
<td>±140</td>
<td>±45</td>
<td>±280</td>
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<tr>
<td></td>
<td>Input Voltage Range</td>
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<td>±10.4</td>
<td>±11.8</td>
<td>±10.4</td>
<td>±11.8</td>
<td>V</td>
</tr>
<tr>
<td>CMRR</td>
<td>Common-Mode Rejection Ratio</td>
<td>( V_{CM} = \pm 10.5V )</td>
<td>●</td>
<td>108</td>
<td>123</td>
<td>102</td>
<td>123</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>( V_S = \pm 4.5V ) to ±18V</td>
<td>●</td>
<td>112</td>
<td>131</td>
<td>106</td>
<td>131</td>
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<tr>
<td>AVOL</td>
<td>Large-Signal Voltage Gain</td>
<td>( R_L \geq 2k, \ V_O = \pm 10V )</td>
<td>●</td>
<td>4.0</td>
<td>20.0</td>
<td>2.5</td>
<td>20.0</td>
</tr>
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<td></td>
<td></td>
<td>( R_L \geq 1k, \ V_O = \pm 10V )</td>
<td>3.0</td>
<td>14.0</td>
<td>2.0</td>
<td>14.0</td>
<td>V/µV</td>
</tr>
<tr>
<td>VOUT</td>
<td>Maximum Output Voltage Swing</td>
<td>( R_L \geq 2k )</td>
<td>●</td>
<td>±11.0</td>
<td>±12.5</td>
<td>±11.0</td>
<td>±12.5</td>
</tr>
<tr>
<td>IS</td>
<td>Supply Current</td>
<td>●</td>
<td>8.5</td>
<td>11.0</td>
<td>8.7</td>
<td>12.5</td>
<td>mA</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

10Hz Voltage Noise Distribution

Wideband Noise, DC to 20kHz

Wideband Voltage Noise (0.1Hz to Frequency Indicated)

Total Noise vs Matched Source Resistance

Total Noise vs Unmatched Source Resistance

Current Noise Spectrum

0.1Hz to 10Hz Voltage Noise

0.01Hz to 1Hz Voltage Noise

Voltage Noise vs Temperature
LT1028/LT1128

TYPICAL PERFORMANCE CHARACTERISTICS

LT1028 Large-Signal Transient Response

LT1028 Small-Signal Transient Response

LT1128 Large-Signal Transient Response

LT1128 Small-Signal Transient Response

Closed-Loop Output Impedance

LT1128

Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor

LT1028

Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor
TYPICAL PERFORMANCE CHARACTERISTICS

Common-Mode Limit Over Temperature

LT1028/LT1128

Common-Mode Rejection Ratio vs Frequency

Power Supply Rejection Ratio vs Frequency

LT1028

Total Harmonic Distortion vs Frequency and Load Resistance

High Frequency Voltage Noise vs Frequency

LT1128

Total Harmonic Distortion vs Closed-Loop Gain

LT1128

Total Harmonic Distortion vs Frequency and Load Resistance

LT1128

Total Harmonic Distortion vs Closed-Loop Gain
Voltage Noise vs Current Noise

The LT1028/LT1128’s less than $1\text{nV/}\sqrt{\text{Hz}}$ voltage noise is three times better than the lowest voltage noise heretofore available (on the LT1007/1037). A necessary condition for such low voltage noise is operating the input transistors at nearly 1mA of collector currents, because voltage noise is inversely proportional to the square root of the collector current. Current noise, however, is directly proportional to the square root of the collector current. Consequently, the LT1028/LT1128’s current noise is significantly higher than on most monolithic op amps.

Therefore, to realize truly low noise performance it is important to understand the interaction between voltage noise ($e_n$), current noise ($I_n$) and resistor noise ($r_n$).

Total Noise vs Source Resistance

The total input referred noise of an op amp is given by

$$e_t = \sqrt{e_n^2 + r_n^2 + (I_n R_{eq})^2}$$

where $R_{eq}$ is the total equivalent source resistance at the two inputs, and

$$r_n = \sqrt{4kT R_{eq}} = 0.13\sqrt{R_{eq}} \text{ in nV/}\sqrt{\text{Hz}} \text{ at } 25^\circ\text{C}$$

As a numerical example, consider the total noise at 1kHz of the gain 1000 amplifier shown below.

\[R_{eq} = 100\Omega + 100\Omega || 100k = 200\Omega\]
\[r_n = 0.13\sqrt{200} = 1.84\text{nV/}\sqrt{\text{Hz}}\]
\[e_n = 0.85\text{nV/}\sqrt{\text{Hz}}\]
\[I_n = 1.0\text{pA/}\sqrt{\text{Hz}}\]
\[e_t = \sqrt{(0.85^2 + 1.84^2 + (1.0 \times 0.2)^2)} = 2.04\text{nV/}\sqrt{\text{Hz}}\]

Output noise = 1000 $e_t = 2.04\mu\text{V/}\sqrt{\text{Hz}}$

At very low source resistance ($R_{eq} < 40\Omega$) voltage noise dominates. As $R_{eq}$ is increased resistor noise becomes the largest term, as in the example above, and the LT1028/LT1128’s voltage noise becomes negligible. As $R_{eq}$ is further increased, current noise becomes important. At 1kHz, when $R_{eq}$ is in excess of 20k, the current noise component is larger than the resistor noise. The total noise versus matched source resistance plot illustrates the above calculations.

The plot also shows that current noise is more dominant at low frequencies, such as 10Hz. This is because resistor noise is flat with frequency, while the 1/f corner of current noise is typically at 250Hz. At 10Hz when $R_{eq} > 1k$, the current noise term will exceed the resistor noise.

When the source resistance is unmatched, the total noise versus unmatched source resistance plot should be consulted. Note that total noise is lower at source resistances below 1k because the resistor noise contribution is less. When $R_S > 1k$ total noise is not improved, however. This is because bias current cancellation is used to reduce input bias current. The cancellation circuitry injects two correlated current noise components into the two inputs. With matched source resistors the injected current noise creates a common-mode voltage noise and gets rejected by the amplifier. With source resistance in one input only, the cancellation noise is added to the amplifier’s inherent noise.

In summary, the LT1028/LT1128 are the optimum amplifiers for noise performance, provided that the source resistance is kept low. The following table depicts which op amp manufactured by Linear Technology should be used to minimize noise, as the source resistance is increased beyond the LT1028/LT1128’s level of usefulness.

**Table: Best Op Amp for Lowest Total Noise vs Source Resistance**

<table>
<thead>
<tr>
<th>SOURCE RESISTANCE(Ω) (Note 1)</th>
<th>AT LOW FREQ(10Hz)</th>
<th>WIDEBAND(1kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 400</td>
<td>LT1028/LT1128</td>
<td>LT1028/LT1128</td>
</tr>
<tr>
<td>400 to 4k</td>
<td>LT1007/1037</td>
<td>LT1028/LT1128</td>
</tr>
<tr>
<td>4k to 40k</td>
<td>LT1001</td>
<td>LT1007/1037</td>
</tr>
<tr>
<td>40k to 500k</td>
<td>LT1012</td>
<td>LT1001</td>
</tr>
<tr>
<td>500k to 5M</td>
<td>LT1012 or LT1055</td>
<td>LT1012</td>
</tr>
<tr>
<td>&gt;5M</td>
<td>LT1055</td>
<td>LT1055</td>
</tr>
</tbody>
</table>

Note 1: Source resistance is defined as matched or unmatched, e.g., $R_S = 1k$ means: 1k at each input, or 1k at one input and zero at the other.
Noise Testing – Voltage Noise

The LT1028/LT1128’s RMS voltage noise density can be accurately measured using the Quan Tech Noise Analyzer, Model 5173 or an equivalent noise tester. Care should be taken, however, to subtract the noise of the source resistor used. Prefabricated test cards for the Model 5173 set the device under test in a closed-loop gain of 31 with a 60Ω source resistor and a 1.8k feedback resistor. The noise of this resistor combination is 0.13√58 = 1.0nV/√Hz. An LT1028/LT1128 with 0.85nV/√Hz noise will read (0.85² + 1.0²)¹/² = 1.31nV/√Hz. For better resolution, the resistors should be replaced with a 10Ω source and 300Ω feedback resistor. Even a 10Ω resistor will show an apparent noise which is 8% to 10% too high.

The 0.1Hz to 10Hz peak-to-peak noise of the LT1028/LT1128 is measured in the test circuit shown. The frequency response of this noise tester indicates that the 0.1Hz corner is defined by only one zero. The test time to measure 0.1Hz to 10Hz noise should not exceed 10 seconds, as this time limit acts as an additional zero to eliminate noise contributions from the frequency band below 0.1Hz.

Measuring the typical 35nV peak-to-peak noise performance of the LT1028/LT1128 requires special test precautions:

(a) The device should be warmed up for at least five minutes. As the op amp warms up, its offset voltage changes typically 10µV due to its chip temperature increasing 30°C to 40°C from the moment the power supplies are turned on. In the 10 second measurement interval these temperature-induced effects can easily exceed tens of nanovolts.

(b) For similar reasons, the device must be well shielded from air current to eliminate the possibility of thermoelectric effects in excess of a few nanovolts, which would invalidate the measurements.

(c) Sudden motion in the vicinity of the device can also “feedthrough” to increase the observed noise.

A noise-voltage density test is recommended when measuring noise on a large number of units. A 10Hz noise-voltage density measurement will correlate well with a 0.1Hz to 10Hz peak-to-peak noise reading since both results are determined by the white noise and the location of the 1/f corner frequency.
Noise Testing – Current Noise

Current noise density \( (I_n) \) is defined by the following formula, and can be measured in the circuit shown:

\[
I_n = \left[ e_{no}^2 - (31 \times 18.4nV/\sqrt{Hz})^2 \right]^{1/2} \frac{20k \times 31}{1.8k}
\]

If the Quan Tech Model 5173 is used, the noise reading is input-referred, therefore the result should not be divided by 31; the resistor noise should not be multiplied by 31.

100% Noise Testing

The 1kHz voltage and current noise is 100% tested on the LT1028/LT1128 as part of automated testing; the approximate frequency response of the filters is shown. The limits on the automated testing are established by extensive correlation tests on units measured with the Quan Tech Model 5173.

10Hz voltage noise density is sample tested on every lot. Devices 100% tested at 10Hz are available on request for an additional charge.

10Hz current noise is not tested on every lot but it can be inferred from 100% testing at 1kHz. A look at the current noise spectrum plot will substantiate this statement. The only way 10Hz current noise can exceed the guaranteed limits is if its 1/f corner is higher than 800Hz and/or its white noise is high. If that is the case then the 1kHz test will fail.
Frequency Response

The LT1028’s Gain, Phase vs Frequency plot indicates that the device is stable in closed-loop gains greater than +2 or −1 because phase margin is about 50° at an open-loop gain of 6dB. In the voltage follower configuration phase margin seems inadequate. This is indeed true when the output is shorted to the inverting input and the noninverting input is driven from a 50Ω source impedance. However, when feedback is through a parallel R-C network (provided CF < 68pF), the LT1028 will be stable because of interaction between the input resistance and capacitance and the feedback network. Larger source resistance at the noninverting input has a similar effect. The following voltage follower configurations are stable:

Unity-Gain Buffer Applications (LT1128 Only)

When RF ≤ 100Ω and the input is driven with a fast, large-signal pulse (>1V), the output waveform will look as shown in the pulsed operation diagram.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With RF ≥ 500Ω, the output is capable of handling the current requirements (I_L ≤ 20mA at 10V) and the amplifier stays in its active mode and a smooth transition will occur.

As with all operational amplifiers when RF > 2k, a pole will be created with RF and the amplifier’s input capacitance, creating additional phase shift and reducing the phase margin. A small capacitor (20pF to 50pF) in parallel with RF will eliminate this problem.
If $C_F$ is only used to cut noise bandwidth, a similar effect can be achieved using the over-compensation terminal. The Gain, Phase plot also shows that phase margin is about 45° at gain of 10 (20dB). The following configuration has a high (≈70%) overshoot without the 10pF capacitor because of additional phase shift caused by the feedback resistor – input capacitance pole. The presence of the 10pF capacitor cancels this pole and reduces overshoot to 5%.

**Over-Compensation**

The LT1028/LT1128 are equipped with a frequency over-compensation terminal (pin 5). A capacitor connected between pin 5 and the output will reduce noise bandwidth. Details are shown on the Slew Rate, Gain-Bandwidth Product vs Over-Compensation Capacitor plot. An additional benefit is increased capacitive load handling capability.

**TYPICAL APPLICATION**

**Strain Gauge Signal Conditioner with Bridge Excitation**

**Low Noise Voltage Regulator**

The LT1028's noise contribution is negligible compared to the bridge noise.
**TYPICAL APPLICATION**

### Paralleling Amplifiers to Reduce Voltage Noise

1. Assume voltage noise of LT1028 and 7.5 Ω source resistor = 0.9 nV/√Hz.
2. Gain with n LT1028s in parallel = \( n \times 200 \).
3. Output noise = \( \sqrt{n} \times 200 \times 0.9 \text{nV}/\sqrt{\text{Hz}} \).
4. Input referred noise = \( \frac{\text{output noise}}{n} = \frac{0.9 \text{nV}/\sqrt{\text{Hz}}}{n} \).
5. Noise current at input increases \( \sqrt{n} \) times.
6. If \( n = 5 \), gain = 1000, bandwidth = 1 MHz, RMS noise, DC to 1 MHz = \( \frac{2 \text{µV}}{\sqrt{5}} = 0.9 \text{ µV} \).

### Phono Preamplifier

![Phono Preamplifier Circuit](image)

### Tape Head Amplifier

![Tape Head Amplifier Circuit](image)

### Low Noise, Wide Bandwidth Instrumentation Amplifier

![Low Noise, Wide Bandwidth Instrumentation Amplifier Circuit](image)

### Gyro Pick-Off Amplifier

![Gyro Pick-Off Amplifier Circuit](image)
Super Low Distortion Variable Sine Wave Oscillator

\[ f = \frac{1}{2\pi RC} \]

WHERE R1C1 = R2C2

LT1052

1VRMS OUTPUT
1.5kHz TO 15kHz

MOUNT 1N4148s IN CLOSE PROXIMITY

TRIM FOR LOWEST DISTORTION

<0.0018% DISTORTION AND NOISE. MEASUREMENT LIMITED BY RESOLUTION OF HP359A DISTORTION ANALYZER

Chopper-Stabilized Amplifier

Low Noise Infrared Detector
C2 = 50pF for LT1028
C2 = 275pF for LT1128
PACKAGE DESCRIPTION  Dimensions in inches (millimeters) unless otherwise noted.

**J8 Package**
8-Lead Ceramic DIP

**N8 Package**
8-Lead Plastic DIP

**S8 Package**
8-Lead Plastic SOIC

**Dimensions in inches (millimeters) unless otherwise noted.**
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic SOL

H Package
8-Lead TO-5 Metal Can

NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND SEATING PLANE.
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